An Ultra-High-Speed GaAs Prescaler Using a Dynamic Frequency Divider

KAZUO OSAFUNE, MEMBER, IEEE, AND KUNIKI OHWADA

Abstract—**A high-speed, low-power-consumption prescaler for a phase lock stable oscillator is designed and fabricated with a GaAs MESFET BFL circuit. The prescaler of a 1/32 frequency divider is composed of a dynamic frequency divider for the prescaler first stage, a newly developed dual-phase signal generator, and master–slave T-type flip-flops for the prescaler post stages. The fabricated 1/32 prescaler operated up to 8.5 GHz at only 540 mW. The 1/2 dynamic frequency divider corresponding to the prescaler first stage shows a maximum operation frequency of 13.2 GHz at only 115 mW.**

I. Introduction

SINCE RECENT progress in GaAs logic IC high-speed operation has been remarkable, application in various fields has proceeded [1]. Regarding a local oscillator circuit for satellite [2] or microwave communication systems, use has been made of GaAs IC's due to their characteristics of high-speed operation, low power consumption, and radiation hardness. A conventional prescaler whose division rate is larger than 32 using a GaAs MESFET operated up to 6.1 GHz [3]. To simplify the configuration of a phase lock loop, to improve phase and frequency stability, and to reduce power consumption, a prescaler operating at higher frequency with lower power is necessary. Consequently, a high-speed, low-power prescaler using GaAs IC's is urgently required.

In this paper, a GaAs ultra-high-speed prescaler using a dynamic frequency divider [4], a newly developed dual-phase signal generator, and master–slave T-type flip-flops is described. The dynamic frequency divider has demonstrated higher speed than the static frequency divider, and the prescaler did not require low-frequency operation, so a dynamic frequency divider has been adopted for the first stage of the prescaler. The dynamic frequency divider has one output, and for a master–slave T-type flip-flop to operate at high speed, dual-phase inputs are necessary. Therefore, a dual-phase signal generator has been adapted as a dynamic frequency divider. As a basic gate, a GaAs BFL using only normally-on FET's is advantageous from the viewpoints of high-speed operation, large operation margin, strong performance against large fan-out, and easy fabrication [5], [6]. Circuit simulations of the prescaler operation are made considering FET gate widths for constructing these circuits. The fabrication process uses a closely spaced electrode structure [7]. The fabricated prescaler operates up to 8.5 GHz at only 540 mW. The 1/2 dynamic frequency divider corresponding to the prescaler first stage demonstrated a maximum operation frequency of 13.2 GHz at only 115 mW. The fabricated yield for a 1/32 prescaler operating at more than 5.4 GHz in the laboratory is as much as 11/26 on one wafer.

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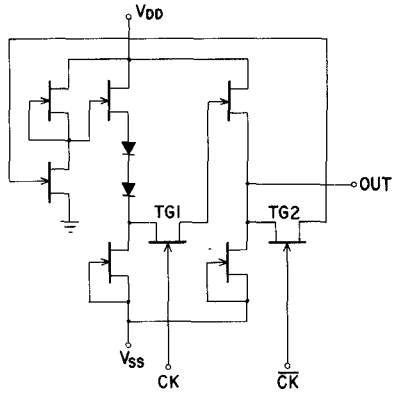

Fig. 1. Circuit schematic diagram of a 1/2 dynamic frequency divider.

II. Circuit Design

A. Dynamic Frequency Divider

The circuit was designed using FET and diode models including parasitic capacitances [8] which were fitted to FET and diode characteristics fabricated by a process that will be described later. The circuit simulations were carried out using SPICE II. FET threshold voltage and the number of level shift diodes were selected as -0.8 V and 2, respectively, in order to obtain high-speed operation and low power consumption [9]. A gate length of 0.7 μm was used because of stable fabrication in the present process.

Fig. 1 shows a circuit schematic diagram of a 1/2 dynamic frequency divider. Here, gate widths of the transmitting gate FET's ($TG1, TG2$) were equal to W_{TGg}, and those of the other FET's and diodes were all 80 μm. The typical bias conditions were $V_{DD} = 3.5$ V and $V_{SS} = -2$ V. Fig. 2 shows a simulated input sensitivity $V_{p\text{-}p}$ versus operating frequency. In this case, the transmitting FET gate widths were $W_{TGg} = 40$ μm, and the phase difference of the two input signals was π. The input sensitivity decreased not only in the higher frequency region but also in the lower frequency region, so the maximum input sensitivity frequency point exists between these frequencies.

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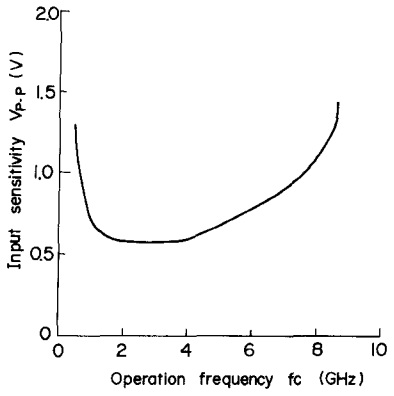

Fig. 2. Simulated input sensitivity V_{p-p} versus operation frequency ($W_{TGg} = 40$ μm, phase difference π).

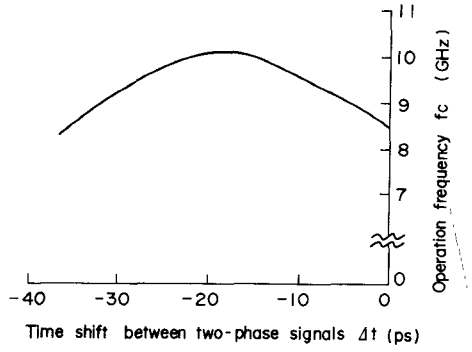

Fig. 3. Simulated relationship between the operation frequency and the time shift of the transmitting gate ($TG2$) input ($W_{TGg} = 40$ μm, $V_{\text{in}p-p} = 1.5$ V).

Fig. 3 shows the simulated relationship between the maximum operation frequency and the time shift (Δt) of the transmitting gate ($TG2$) input from π versus the transmitting gate ($TG1$) input. In this case, the input voltage was 1.5 V_{p-p}. The time shift moved toward minus, and the operation frequency increased and then decreased. Hence, an optimum time shift for operation at maximum frequency exists [4]. Fig. 4 shows the simulated relationship between the maximum operation frequency and the transmitting gate FET gate width (W_{TGg}). In this case, two input signals of the 1/2 dynamic frequency divider were completely shifted by π, and the input voltage was 1.5 V_{p-p}. In the narrower FET gate width region, the operation frequency decreased rapidly, and in the wider FET gate width region, the operation frequency decreased gradually. So, the optimum transmitting gate FET gate width for operation at maximum frequency is around 40 μm [4]. We adopt two transmitting gate FET gate widths of 30 μm and 45 μm for the fabricated 1/2 dynamic frequency dividers, and 45 μm for the fabricated 1/32 prescaler.

B. Dual-Phase Signal Generator and Static Frequency Divider

Fig. 5 shows a circuit schematic diagram of a newly developed dual-phase signal generator. Dual-phase signal outputs whose phases differ by π where used for driving a static master–slave T-type flip-flop frequency divider. The

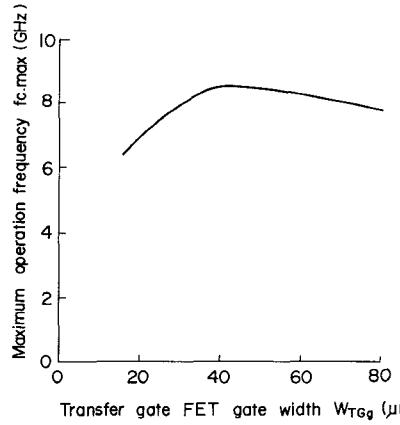

Fig. 4. Simulated relationship between the operation frequency and the transmitting FET gate width ($V_{\text{in}p-p} = 1.5$ V, phase difference $= \pi$).

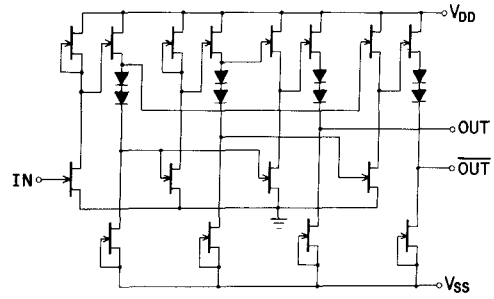

Fig. 5. Circuit schematic diagram of a newly developed dual-phase signal generator.

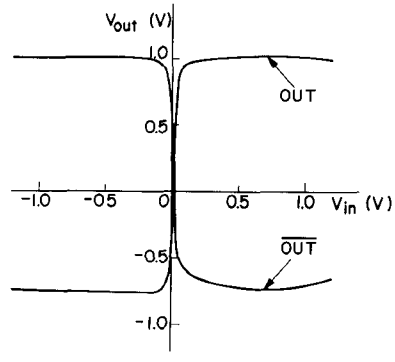

Fig. 6. Simulated transfer characteristics of a dual-phase signal generator.

circuit consists of four BFL basic gates connected at proper level shift positions, and a super buffer circuit construction was used to obtain dual-phase signals. The switching circuit FET gate widths were 40 μm, and the source follower FET and diode gate widths were 80 μm. Fig. 6 shows the simulated transfer characteristics. Sufficiently good transfer characteristics were obtained owing to the above-mentioned special circuit ideas. Fig. 7 shows simulated output characteristics of the dual-phase signal generator and the input sensitivity of the static frequency divider. In this case, the input of a dual-phase signal generator, which was the output of a dynamic frequency divider, was 0.52 V_{p-p}, and the FET and diode gate widths of a static frequency divider were 30 μm. In this figure, the

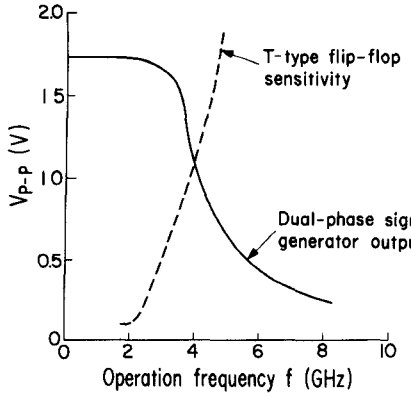

Fig. 7. Simulated output characteristics of a dual-phase signal generator and input sensitivity of a 1/2 static frequency divider.

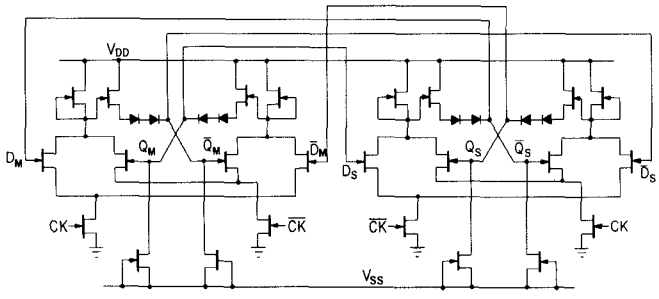

Fig. 8. Circuit schematic diagram of a static master–slave T-type flip-flop.

maximum operation frequency of a static frequency divider was less than 4.0 GHz. Fig. 8 shows a circuit schematic diagram of a static master–slave T-type flip-flop with gate widths of W_g.

C. 1/32 Prescaler

Fig. 9 shows a total block diagram of a 1/32 prescaler. The first stage was the previously described dynamic frequency divider with a transmitting gate FET gate width of 45 μm, and the newly developed dual-phase signal generator followed. The second stage was the static frequency divider with FET and diode gate widths of 30 μm, and the third stage was a static frequency divider with FET and diode gate widths of 10 μm to obtain operation above 2.0 GHz [10]. After the third stage, static frequency dividers with FET and diode gate widths of 10 μm were used to obtain stable operation. The total gate number of a 1/32 prescaler was 42 converting with NOR gates.

III. IC Fabrication

A 2-in-diameter GaAs wafer was used, and the fabrication process used was the closely spaced electrode structure [7]. An active layer was formed by ion implantation. The FET gate length was 0.7 μm, the fabricated FET average threshold voltage V_t across a 2-in-diameter wafer was -0.8 V, and the standard deviation was 101 mV. The FET average transconductance g_m was 137 mS/mm ($V_{GS} = 0$ V, $V_{DS} = 2$ V), the standard deviation, 8.5 mS/mm, and the average drain conductance, 14 mS/mm. Chip sizes of the fabricated prescaler and the 1/2 dynamic frequency

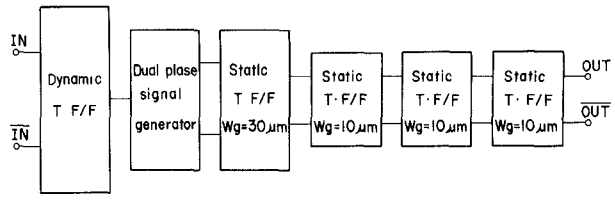

Fig. 9. Total block diagram of a 1/32 prescaler.

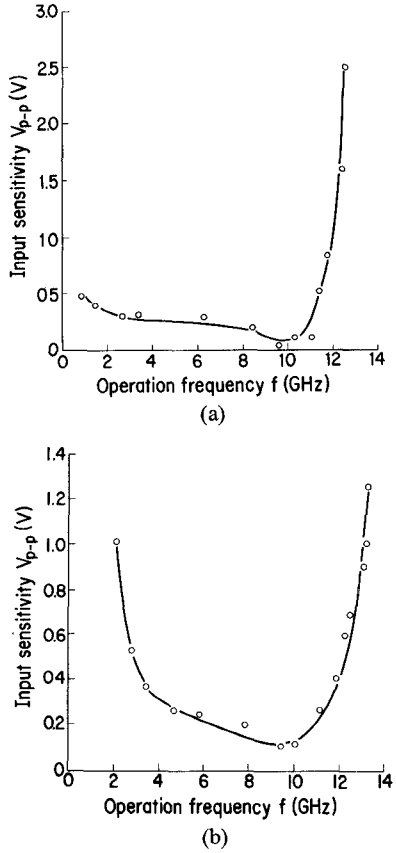

Fig. 10. Input sensitivity V_{p-p} versus operation frequency of a 1/2 dynamic frequency divider. (a) Transmitting gate FET gate width of 30 μm. (b) Transmitting gate FET gate width of 45 μm.

divider were 2.4×1.2 mm square and 0.8×0.9 mm square, respectively. In addition, we fabricated 1/2 static frequency dividers with a gate width of 40 μm, and 17-stage ring oscillators with gate widths of 80 μm and 20 μm. These circuit geometries were optimized and made compact by symmetric circuit arrangements and short interconnection.

IV. Performance

A. Dynamic Frequency Divider

Propagation delay times of fabricated 17-stage ring oscillators with gate widths of 80 μm and 20 μm were 43 ps/gate at 44 mW/gate and 56 ps/gate at 12 mW/gate, respectively. These results corresponded to simulation results calculated from the above-mentioned circuit simulation models considering pattern effects. Fig. 10(a) shows the input sensitivity V_{p-p} versus operation frequency of the fabricated 1/2 dynamic frequency divider of a transmitting gate FET with gate width of 30 μm. The maximum operation frequency was 12.5 GHz, and the minimum

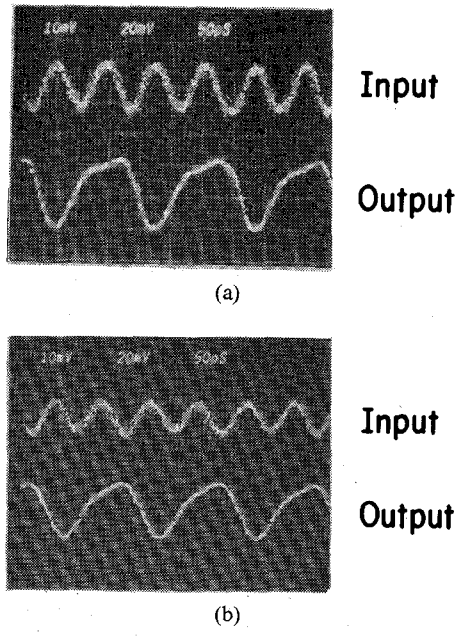

Fig. 11. Maximum operation waveforms of 1/2 dynamic frequency dividers. (a) Waveforms at 12.7 GHz in the case of a transmitting gate FET gate width of 30 μm (input: 37 dB att., output: 6 dB att.). (b) Waveforms at 13.2 GHz in the case of a transmitting gate FET gate width of 45 μm (input: 45 dB att., output: 7 dB att.).

operation frequency 900 MHz; the power consumption was only 105 mW. Fig. 10(b) also shows the input sensitivity V_{p-p} versus operation frequency of the fabricated 1/2 dynamic frequency divider with a transmitting gate FET gate width of 45 μm. The maximum operation frequency was 13.2 GHz, the minimum operation frequency was 2.1 GHz, and the power consumption was only 115 mW. In these cases, two input signal phases were optimized as shown in Fig. 3. These results almost corresponded to the simulated results.

The operation waveforms for transmitting gate FET gate widths of 30 μm and 45 μm are shown in Fig. 11. Output waveforms were measured into a 50-Ω load. Fig. 11(a) shows the waveforms at 12.7 GHz in the case of a transmitting gate FET with gate width of 30 μm. Fig. 11(b) shows waveforms at 13.2 GHz of a transmitting gate FET with gate width of 45 μm. The latter maximum operation frequency was the highest frequency by a digital semiconductor IC reported to date [11].

The maximum operation frequency of a 1/2 static frequency divider by dual-phase with an FET gate width of 40 μm was 4.8 GHz at 84 mW, using the same process. These results are summarized in Table I. It is clear that in the same power consumption condition, a dynamic frequency divider has 2.5 times the speed of a static frequency divider.

B. 1/32 Prescaler

Fig. 12 shows the input sensitivity V_{p-p} versus operation frequency of the fabricated 1/32 prescaler, where a dynamic frequency divider transmitting gate FET with gate width of 45 μm was used. The maximum operation frequency was 8.5 GHz; the minimum was 2.1 GHz; and

TABLE I
COMPARISON OF DYNAMIC FREQUENCY DIVIDERS AND STATIC FREQUENCY DIVIDERS

		Maximum Operation Freq.	Power Consumption
Dynamic Divider (Wg=80μm)	W_{Tgg}=30μm	12.7 GHz	105 mW
	45	13.2	115
Static Divider	Wg=40μm	4.8	84

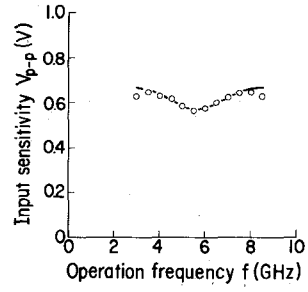

Fig. 12. Input sensitivity V_{p-p} versus operation frequency of a 1/32 prescaler.

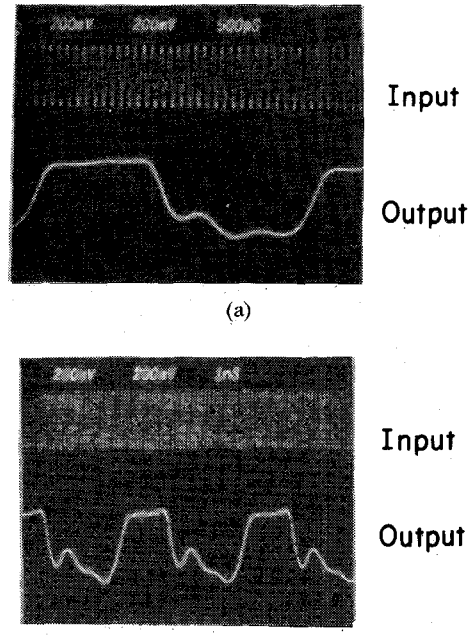

Fig. 13. Operation waveforms of a 1/32 prescaler. (a) Waveforms at 8.0 GHz. (b) Waveforms at 8.4 GHz.

the power consumption was only 540 mW. In this case, two input signal phases were optimized. From this result, it was clear that the maximum operation frequency was limited by the dual-phase signal generator output characteristics, as shown in Fig. 7.

The operation waveforms of the 1/32 prescaler are shown in Fig. 13. Fig. 13(a) shows the waveforms at 8.0 GHz, and Fig. 13(b) shows the waveforms at 8.4 GHz, in good agreement with the simulated result. The fabrication yield for a 1/32 prescaler to operate at more than 5.4 GHz in the laboratory was as much as 11/26 on one wafer. And the fabrication yield for a 1/2 dynamic frequency divider to operate at more than 12.4 GHz was 4/4.

V. Conclusions

A 1/32 prescaler used to stabilize a local oscillator circuit in satellite and microwave communication systems was designed and fabricated using a GaAs MESFET BFL circuit which gives high-speed operation and large operation margin. We designed the high-speed and low-power-consumption prescaler using a dynamic frequency divider, a new dual-phase signal generator, and master–slave T-type flip-flops, giving consideration to FET gate widths used in constructing these circuits. The fabrication process used was the closely spaced electrode structure. The fabricated prescaler operated up to 8.5 GHz at only 540 mW. The corresponding 1/2 dynamic frequency divider showed a maximum operation frequency of 13.2 GHz at only 115 mW, which is the highest operation frequency by a digital semiconductor IC reported to date. The fabrication yield for a 1/32 prescaler to operate at more than 5.4 GHz in the laboratory was as much as 11/26 on one wafer.

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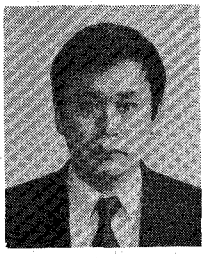

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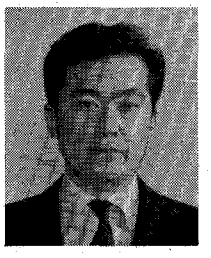

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